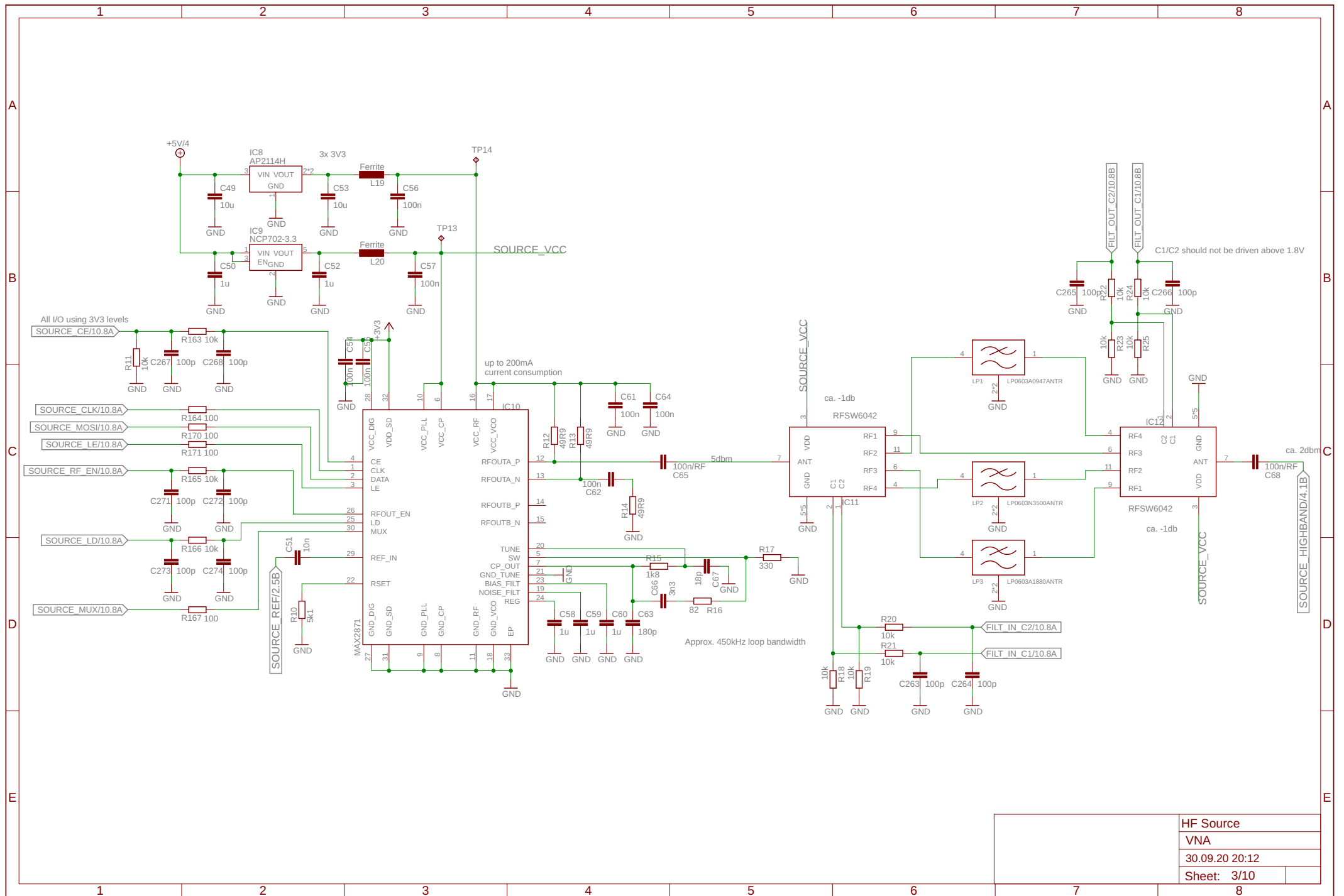
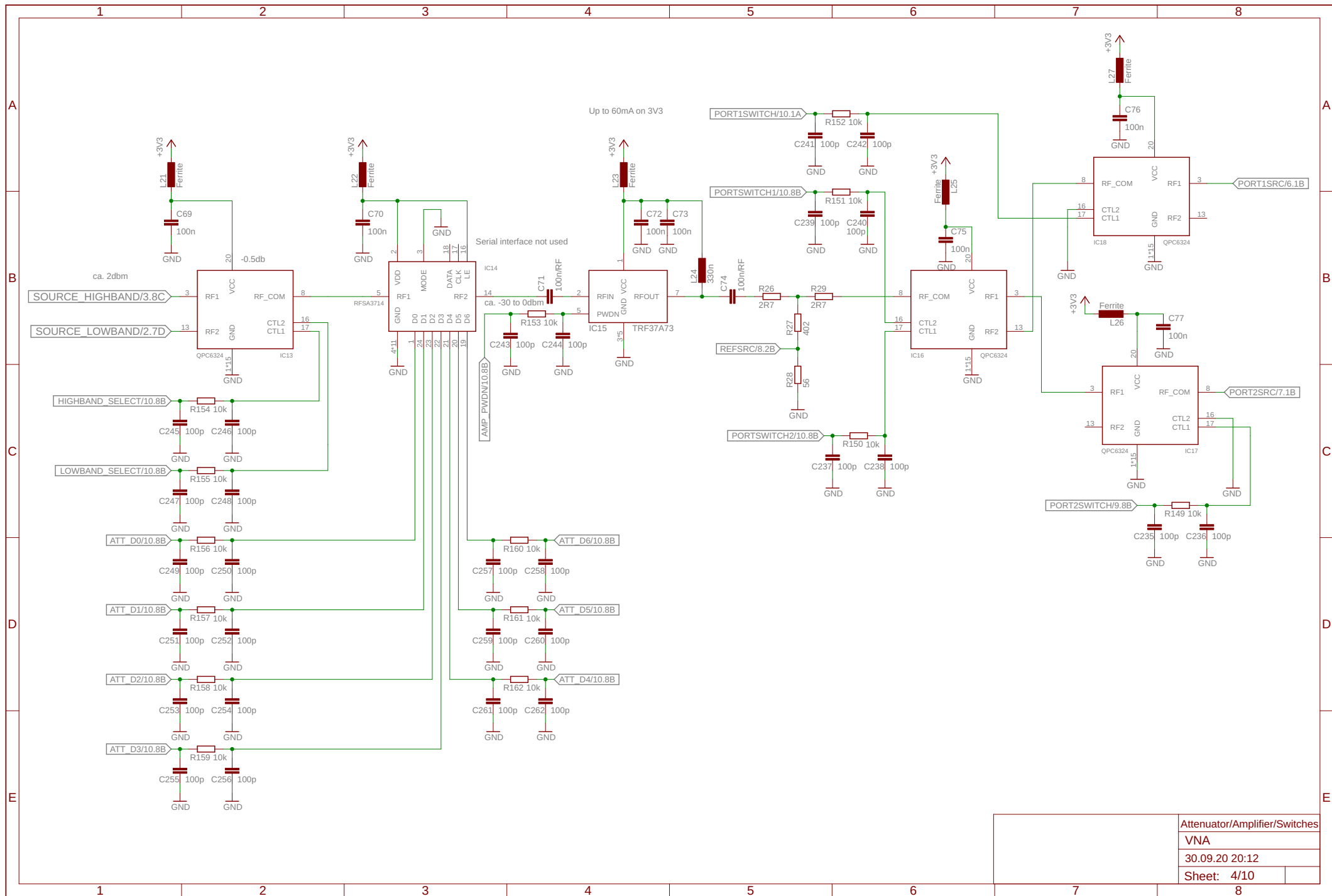


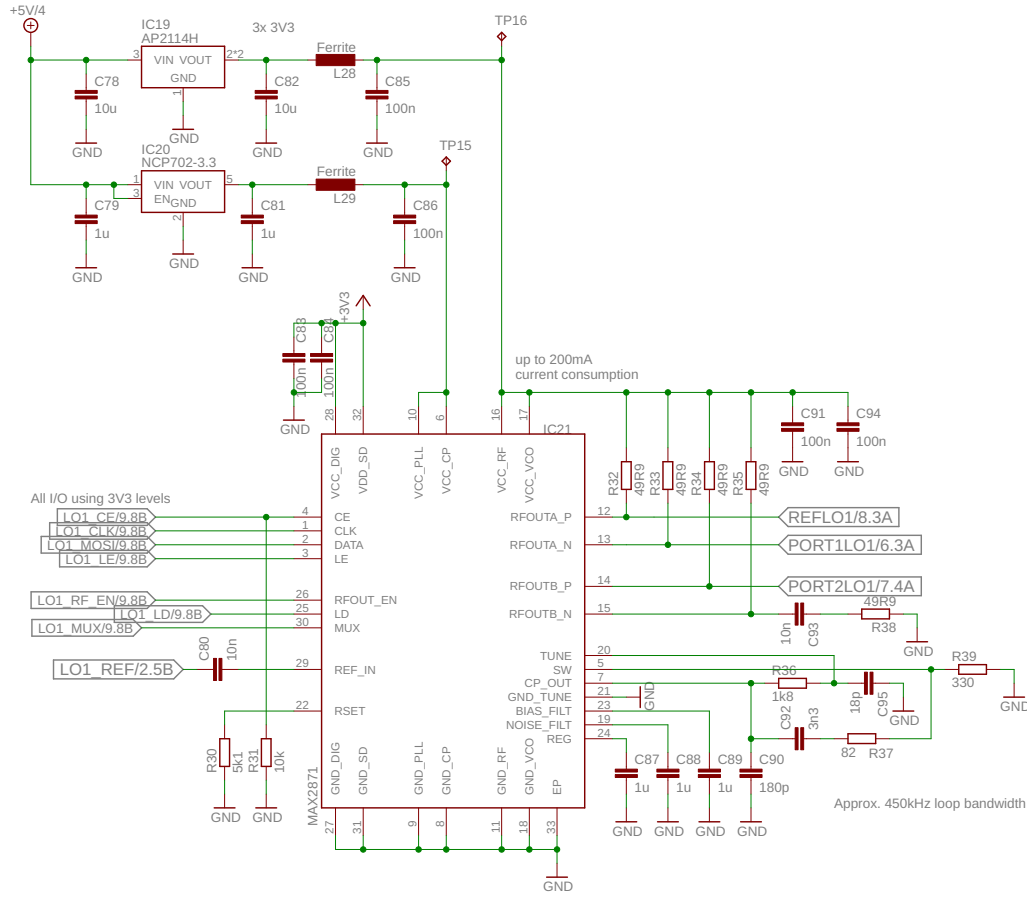
40MHz lowpass

Reference CLK and 2.LO
VNA
30.09.20 20:12
Sheet: 2/10

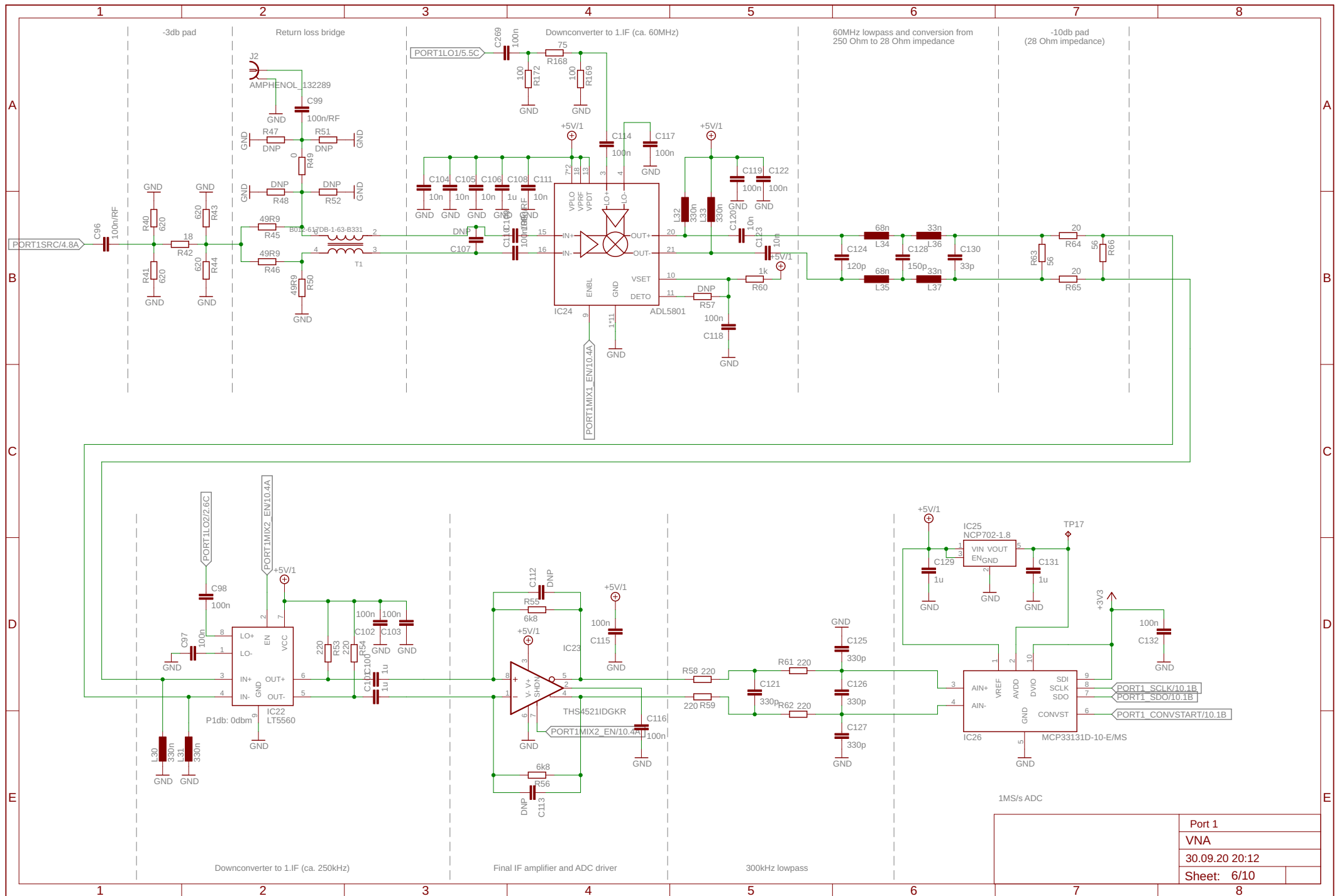


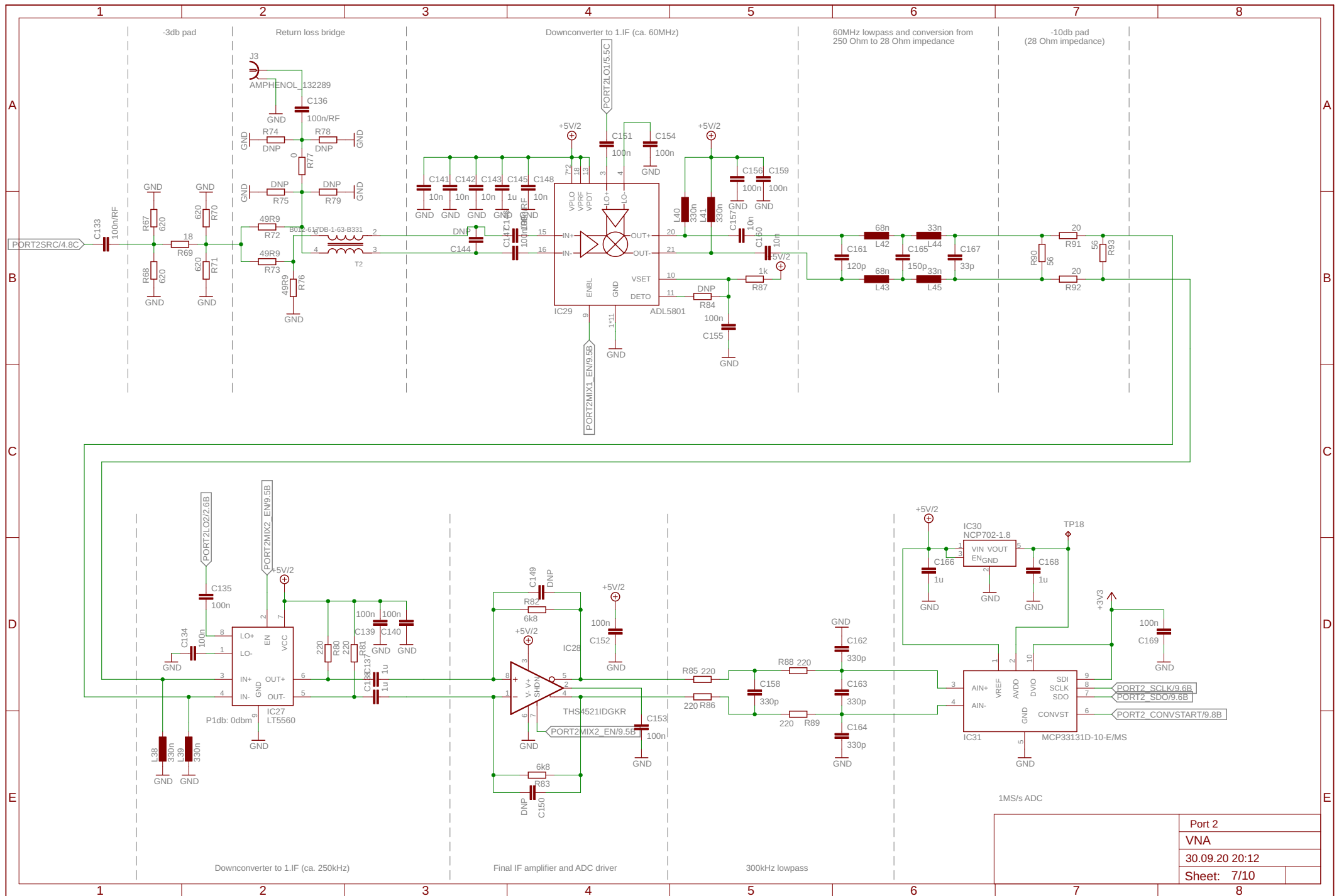
HF Source
VNA
30.09.20 20:12
Sheet: 3/10



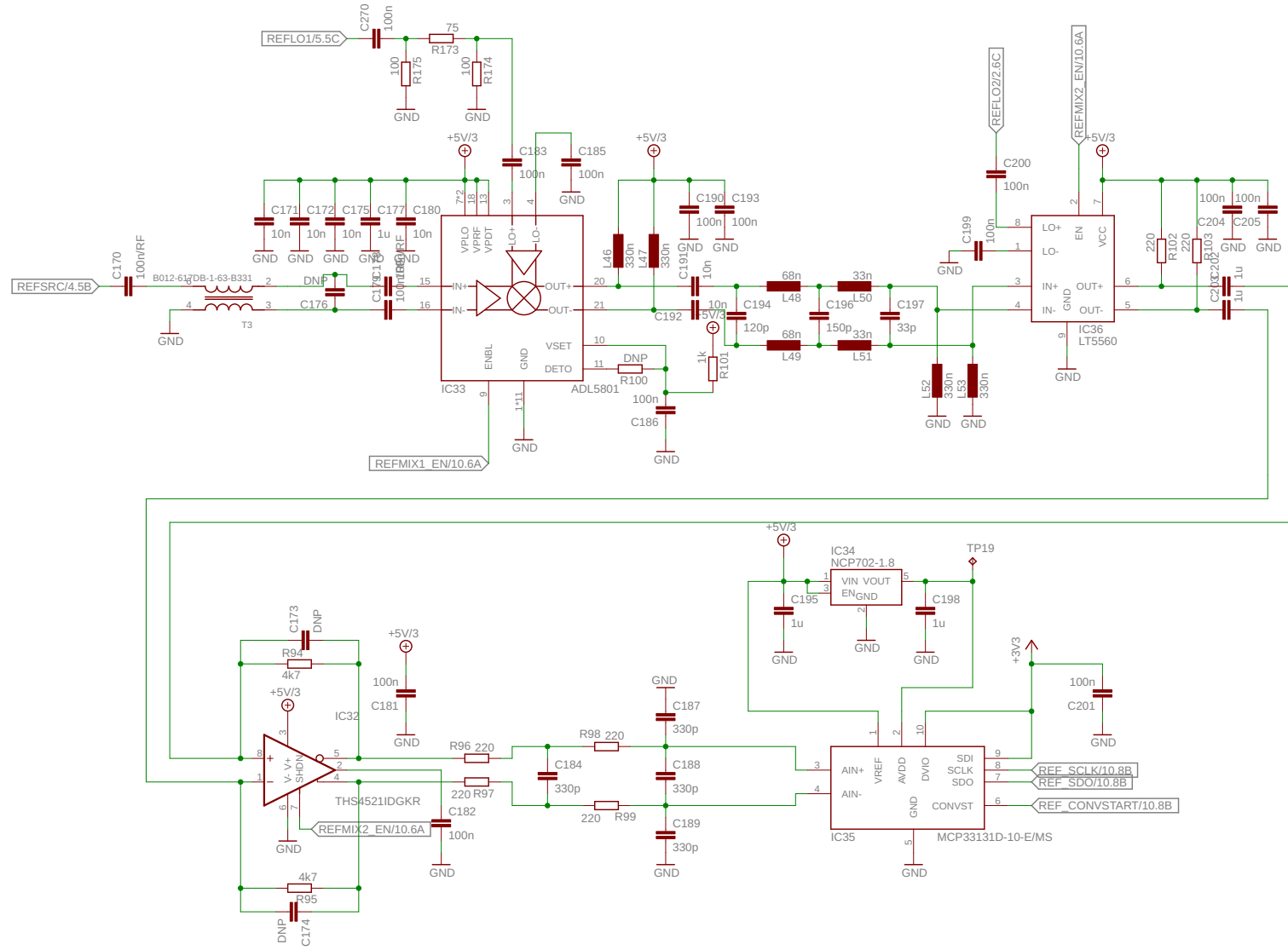


1.LO	
VNA	
30.09.20 20:12	
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Port 2
VNA
30.09.20 20:12
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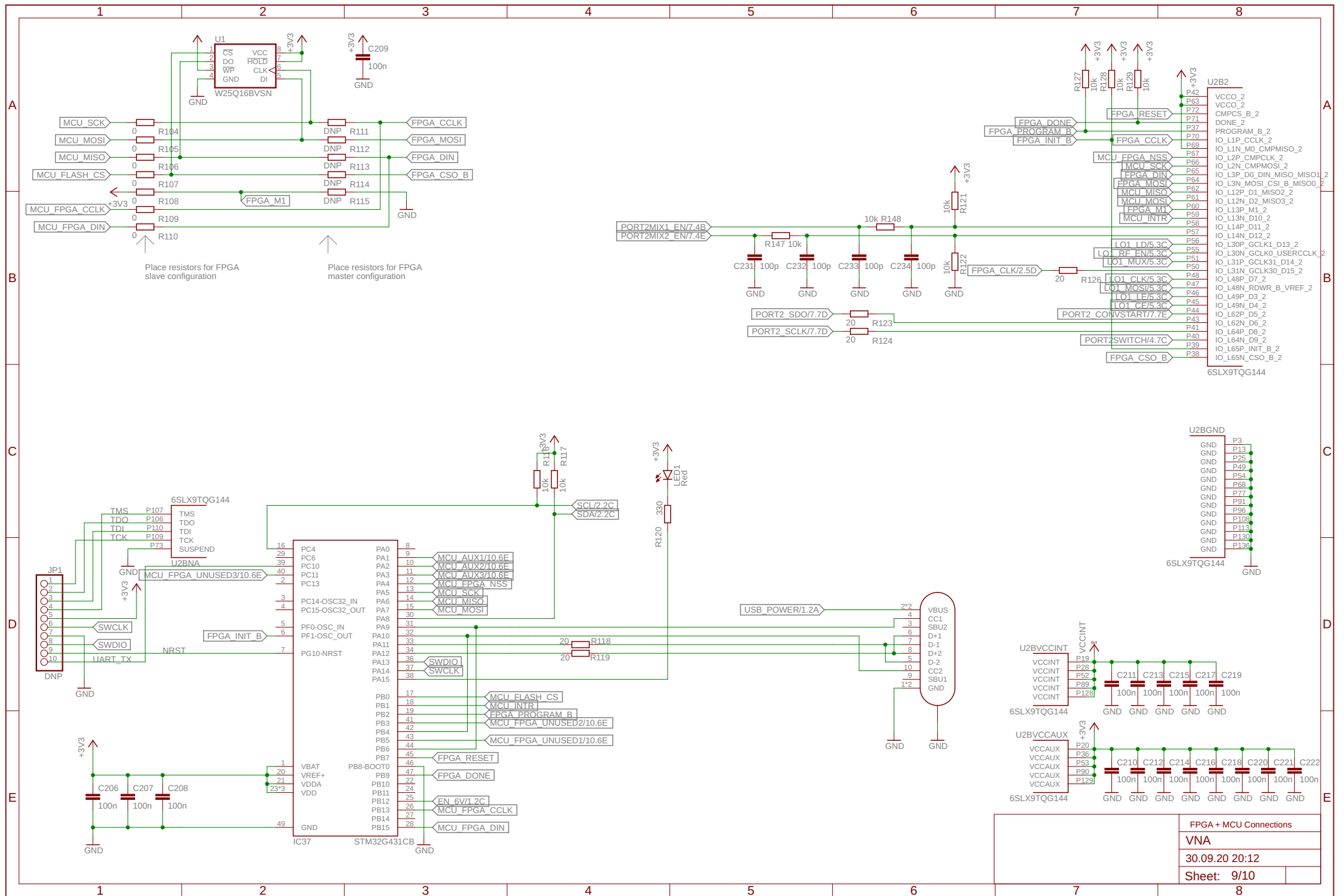


Reference Signal

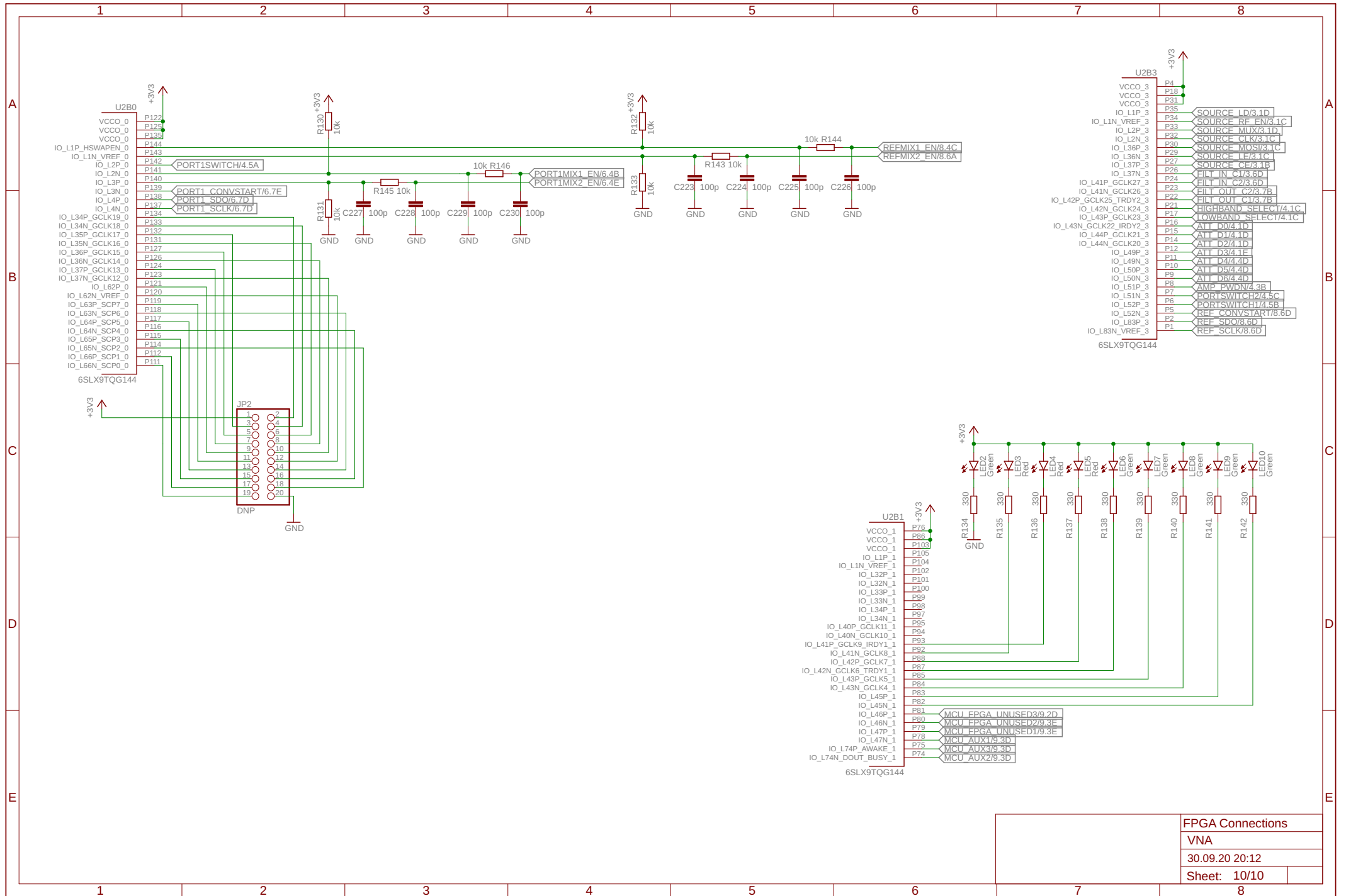
VNA

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FPGA + MCU Connections	
VNA	
30.09.20 20:12	
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FPGA Connections

VNA
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