



## 1. Description

### 1.1. Project

Project Name	STM32G474RETx_Demo_Blink
Board Name	NUCLEO-G474RE
Generated with:	STM32CubeMX 6.11.1
Date	07/28/2024

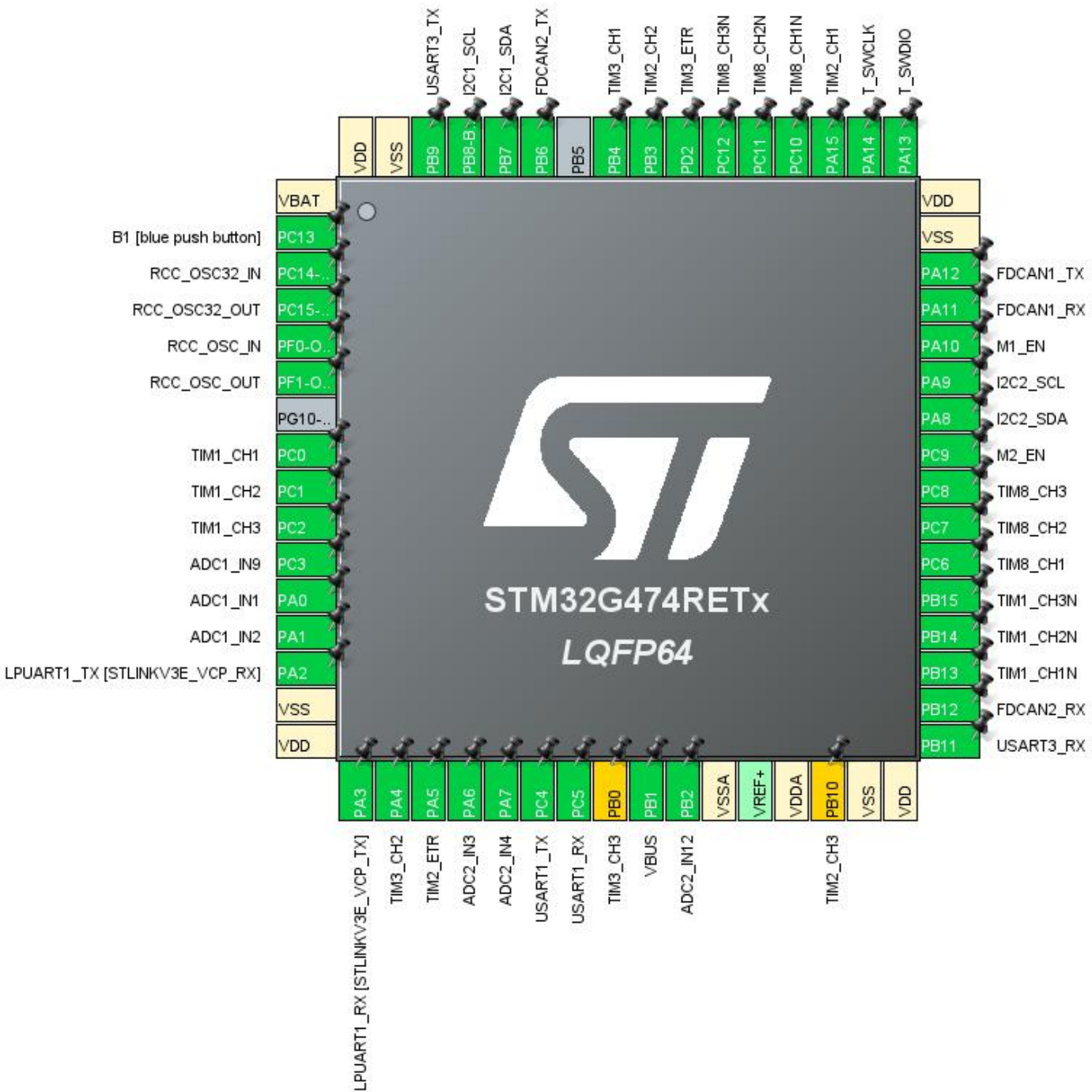
### 1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G474RETx
MCU Package	LQFP64
MCU Pin number	64

### 1.3. Core(s) information

Core(s)	ARM Cortex-M4
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## 2. Pinout Configuration



### 3. Pins Configuration

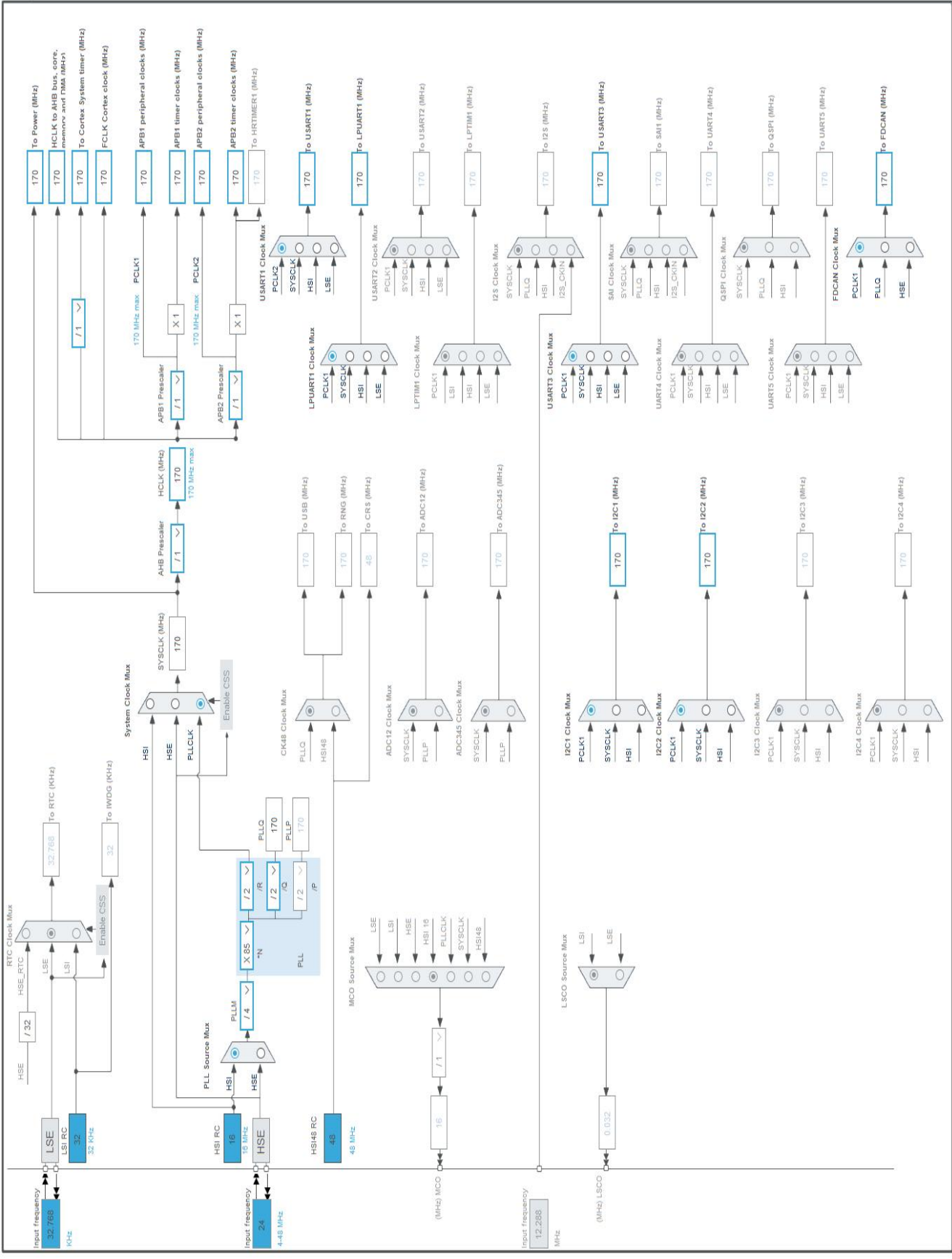
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [blue push button]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
8	PC0	I/O	TIM1_CH1	
9	PC1	I/O	TIM1_CH2	
10	PC2	I/O	TIM1_CH3	
11	PC3	I/O	ADC1_IN9	
12	PA0	I/O	ADC1_IN1	
13	PA1	I/O	ADC1_IN2	
14	PA2	I/O	LPUART1_TX	LPUART1_TX [STLINKV3E_VCP_RX]
15	VSS	Power		
16	VDD	Power		
17	PA3	I/O	LPUART1_RX	LPUART1_RX [STLINKV3E_VCP_TX]
18	PA4	I/O	TIM3_CH2	
19	PA5	I/O	TIM2_ETR	
20	PA6	I/O	ADC2_IN3	
21	PA7	I/O	ADC2_IN4	
22	PC4	I/O	USART1_TX	
23	PC5	I/O	USART1_RX	
24	PB0 *	I/O	TIM3_CH3	
25	PB1	I/O	ADC3_IN1	VBUS
26	PB2	I/O	ADC2_IN12	
27	VSSA	Power		
29	VDDA	Power		
30	PB10 *	I/O	TIM2_CH3	
31	VSS	Power		
32	VDD	Power		
33	PB11	I/O	USART3_RX	
34	PB12	I/O	FDCAN2_RX	
35	PB13	I/O	TIM1_CH1N	
36	PB14	I/O	TIM1_CH2N	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PB15	I/O	TIM1_CH3N	
38	PC6	I/O	TIM8_CH1	
39	PC7	I/O	TIM8_CH2	
40	PC8	I/O	TIM8_CH3	
41	PC9 **	I/O	GPIO_Output	M2_EN
42	PA8	I/O	I2C2_SDA	
43	PA9	I/O	I2C2_SCL	
44	PA10 **	I/O	GPIO_Output	M1_EN
45	PA11	I/O	FDCAN1_RX	
46	PA12	I/O	FDCAN1_TX	
47	VSS	Power		
48	VDD	Power		
49	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
50	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK
51	PA15	I/O	TIM2_CH1	
52	PC10	I/O	TIM8_CH1N	
53	PC11	I/O	TIM8_CH2N	
54	PC12	I/O	TIM8_CH3N	
55	PD2	I/O	TIM3_ETR	
56	PB3	I/O	TIM2_CH2	
57	PB4	I/O	TIM3_CH1	
59	PB6	I/O	FDCAN2_TX	
60	PB7	I/O	I2C1_SDA	
61	PB8-BOOT0	I/O	I2C1_SCL	
62	PB9	I/O	USART3_TX	
63	VSS	Power		
64	VDD	Power		

\*\* The pin is affected with an I/O function

\* The pin is affected with a peripheral function but no peripheral mode is activated

# 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	STM32G474RETx_Demo_Blink
Project Folder	C:\Users\Michael_Chemic\Desktop\STM32G4-DRV8301-FOC
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_G4 V1.5.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_LPUART1_UART_Init	LPUART1
5	MX_USART1_UART_Init	USART1
6	MX_TIM1_Init	TIM1
7	MX_TIM8_Init	TIM8
8	MX_ADC1_Init	ADC1
9	MX_ADC2_Init	ADC2
10	MX_I2C1_Init	I2C1
11	MX_I2C2_Init	I2C2

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Rank	Function Name	Peripheral Instance Name
12	MX_USART3_UART_Init	USART3
13	MX_FDCAN1_Init	FDCAN1
14	MX_ADC3_Init	ADC3
15	MX_FDCAN2_Init	FDCAN2
16	MX_TIM2_Init	TIM2
17	MX_TIM3_Init	TIM3



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
MCU	STM32G474RETx
Datasheet	DS12288_Rev0

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

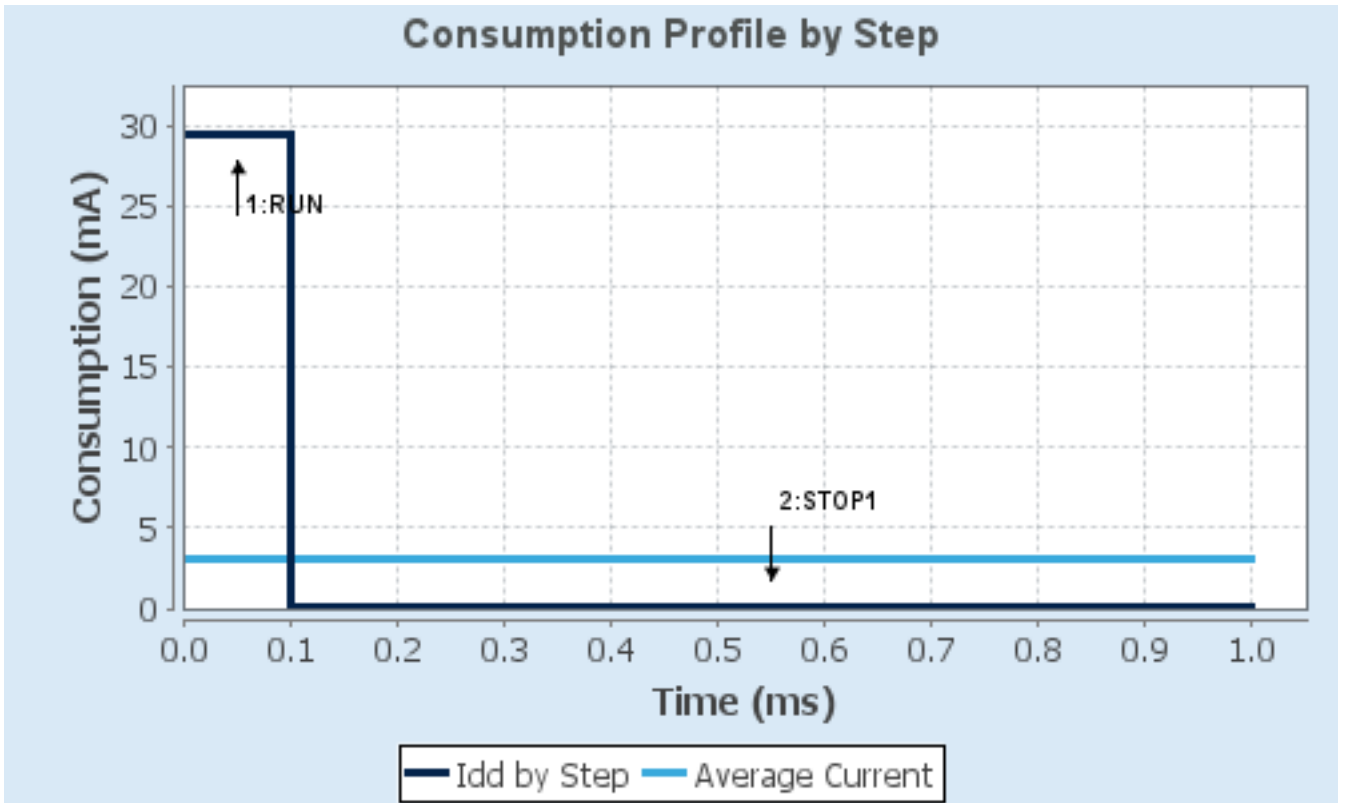
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP1
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Range1-Boost	NoRange
<b>Fetch Type</b>	FLASH/DualBank/ART	NA
<b>CPU Frequency</b>	170 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	ALL CLOCKS OFF
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	29.5 mA	80.5 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	213.0	0.0
<b>Ta Max</b>	124.25	129.98
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	3.02 mA
Battery Life	1 month, 16 days, 9 hours	Average DMIPS	212.5 DMIPS

#### 1.6. Chart



## 2. Peripherals and Middlewares Configuration

### 2.1. ADC1

**IN1: IN1 Single-ended**

**IN2: IN2 Single-ended**

**IN9: IN9 Single-ended**

#### 2.1.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Clock Prescaler Synchronous clock mode divided by 4

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Gain Compensation 0

Scan Conversion Mode Enabled

End Of Conversion Selection End of single conversion

Low Power Auto Wait Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode **Enabled \***

Number Of Discontinuous Conversions 1

DMA Continuous Requests Disabled

Overrun behaviour Overrun data preserved

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion **3 \***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 1

Sampling Time 2.5 Cycles

Offset Number No offset

Rank **2 \***

Channel **Channel 2 \***

Sampling Time 2.5 Cycles

Offset Number No offset

Rank **3 \***

Channel **Channel 9 \***

Sampling Time 2.5 Cycles

Offset Number No offset

**ADC\_Injected\_ConversionMode:**

Enable Injected Conversions Disable

**Analog Watchdog 1:**

Enable Analog WatchDog1 Mode false

**Analog Watchdog 2:**

Enable Analog WatchDog2 Mode false

**Analog Watchdog 3:**

Enable Analog WatchDog3 Mode false

**2.2. ADC2**

**IN3: IN3 Single-ended**

**IN4: IN4 Single-ended**

**IN12: IN12 Single-ended**

2.2.1. Parameter Settings:

**ADCs\_Common\_Settings:**

Mode Independent mode

**ADC\_Settings:**

Clock Prescaler Synchronous clock mode divided by 4

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Gain Compensation 0

Scan Conversion Mode Enabled

End Of Conversion Selection End of single conversion

Low Power Auto Wait Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode **Enabled \***

Number Of Discontinuous Conversions 1

DMA Continuous Requests Disabled

Overrun behaviour Overrun data preserved

**ADC\_Regular\_ConversionMode:**

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion **3 \***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 3

Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>2 *</b>
Channel	<b>Channel 4 *</b>
Sampling Time	2.5 Cycles
Offset Number	No offset
<u>Rank</u>	<b>3 *</b>
Channel	<b>Channel 12 *</b>
Sampling Time	2.5 Cycles
Offset Number	No offset

**ADC\_Injected\_ConversionMode:**

Enable Injected Conversions      Disable

**Analog Watchdog 1:**

Enable Analog WatchDog1 Mode      false

**Analog Watchdog 2:**

Enable Analog WatchDog2 Mode      false

**Analog Watchdog 3:**

Enable Analog WatchDog3 Mode      false

**2.3. ADC3**

**mode: IN1**

2.3.1. Parameter Settings:

**ADCs\_Common\_Settings:**

Mode      Independent mode

**ADC\_Settings:**

Clock Prescaler      Synchronous clock mode divided by 4

Resolution      ADC 12-bit resolution

Data Alignment      Right alignment

Gain Compensation      0

Scan Conversion Mode      Disabled

End Of Conversion Selection      End of single conversion

Low Power Auto Wait      Disabled

Continuous Conversion Mode      **Enabled \***

Discontinuous Conversion Mode      Disabled

DMA Continuous Requests      Disabled

Overrun behaviour      Overrun data preserved

**ADC\_Regular\_ConversionMode:**

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset

**ADC\_Injected\_ConversionMode:**

Enable Injected Conversions	Disable
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**Analog Watchdog 1:**

Enable Analog WatchDog1 Mode	false
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**Analog Watchdog 2:**

Enable Analog WatchDog2 Mode	false
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**Analog Watchdog 3:**

Enable Analog WatchDog3 Mode	false
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## 2.4. FDCAN1

### mode: Activated

#### 2.4.1. Parameter Settings:

**Basic Parameters:**

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Sync Jump Width	1
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Std Filters Nbr	0
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

**Bit Timings Parameters:**

Nominal Prescaler	16
Nominal Time Quantum	

	<b>94.11764705882354 *</b>
Nominal Time Seg1	2
Nominal Time Seg2	2
Nominal Time for one Bit	<b>470 *</b>
Nominal Baud Rate	<b>2125000 *</b>

## 2.5. FDCAN2

**mode: Activated**

### 2.5.1. Parameter Settings:

#### **Basic Parameters:**

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Sync Jump Width	1
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Std Filters Nbr	0
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

#### **Bit Timings Parameters:**

Nominal Prescaler	16
Nominal Time Quantum	<b>94.11764705882354 *</b>
Nominal Time Seg1	2
Nominal Time Seg2	2
Nominal Time for one Bit	<b>470 *</b>
Nominal Baud Rate	<b>2125000 *</b>

## 2.6. I2C1

**I2C: I2C**

### 2.6.1. Parameter Settings:



**Timing configuration:**

Custom Timing	Disabled
I2C Speed Mode	<b>Fast Mode Plus *</b>
I2C Speed Frequency (KHz)	1000
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	<b>0x00802172 *</b>

**Slave Features:**

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

## 2.7. I2C2

### I2C: I2C

#### 2.7.1. Parameter Settings:

**Timing configuration:**

Custom Timing	Disabled
I2C Speed Mode	<b>Fast Mode Plus *</b>
I2C Speed Frequency (KHz)	1000
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	<b>0x00802172 *</b>

**Slave Features:**

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

## 2.8. LPUART1

### Mode: Asynchronous

#### 2.8.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	209700
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

##### Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 2.9. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator

### Low Speed Clock (LSE) : Crystal/Ceramic Resonator

#### 2.9.1. Parameter Settings:

##### System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

##### RCC Parameters:

HSI Calibration Value	64
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HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
<b>Power Parameters:</b>	
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost
<b>Peripherals Clock Configuration:</b>	
Generate the peripherals clock configuration	TRUE

## 2.10. SYS

**Debug: Serial Wire**

**Timebase Source: SysTick**

**mode: save power of non-active UCPD - deactive Dead Battery pull-up**

## 2.11. TIM1

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1 CH1N**

**Channel2: PWM Generation CH2 CH2N**

**Channel3: PWM Generation CH3 CH3N**

### 2.11.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value )	<b>5499 *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

#### **Break And Dead Time management - BRK Configuration:**

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable

- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

**Break And Dead Time management - BRK2 Configuration:**

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

**Break And Dead Time management - Output Configuration:**

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
DeadTime Preload	Disable
Dead Time	0
Asymmetrical DeadTime	Disable
Falling Dead Time	0

**Clear Input:**

Clear Input Source	Disable
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**PWM Generation Channel 1 and 1N:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

**PWM Generation Channel 2 and 2N:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>500 *</b>

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

### **PWM Generation Channel 3 and 3N:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

## **2.12. TIM2**

### **Combined Channels: Encoder Mode + index**

#### 2.12.1. Parameter Settings:

##### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 32 bits value )	<b>4095 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

##### **Encoder:**

Index input polarity	Non Inverted
Index Prescaler	Capture performed each event
index filter	0
encoder first index	Disable
Index Position	Encoder index position is AB=00
Index Direction	Index resets the counter whatever the direction
Encoder Mode	<b>Encoder Mode TI1 and TI2 *</b>
Slave Mode Preload Activation	Disable

\_\_\_\_ Parameters for Channel 1 \_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

\_\_\_\_ Parameters for Channel 2 \_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

## 2.13. TIM3

### Combined Channels: Encoder Mode + index

#### 2.13.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value )	<b>4095 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

##### Encoder:

Index input polarity	Non Inverted
Index Prescaler	Capture performed each event
index filter	0
encoder first index	Disable
Index Position	Encoder index position is AB=00
Index Direction	Index resets the counter whatever the direction
Encoder Mode	<b>Encoder Mode TI1 and TI2 *</b>

Slave Mode Preload Activation	Disable
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\_\_\_\_ Parameters for Channel 1 \_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

\_\_\_\_ Parameters for Channel 2 \_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

## 2.14. TIM8

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1 CH1N**

**Channel2: PWM Generation CH2 CH2N**

**Channel3: PWM Generation CH3 CH3N**

### 2.14.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value )	<b>5499 *</b>
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

#### **Break And Dead Time management - BRK Configuration:**

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

#### **Break And Dead Time management - BRK2 Configuration:**

BRK2 State	Disable
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BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable
- COMP4	Disable
- COMP5	Disable
- COMP6	Disable
- COMP7	Disable

**Break And Dead Time management - Output Configuration:**

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
DeadTime Preload	Disable
Dead Time	0
Asymmetrical DeadTime	Disable
Falling Dead Time	0

**Clear Input:**

Clear Input Source	Disable
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**PWM Generation Channel 1 and 1N:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

**PWM Generation Channel 2 and 2N:**

Mode	PWM mode 1
Pulse (16 bits value)	<b>500 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

**PWM Generation Channel 3 and 3N:**

Mode	PWM mode 1
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Pulse (16 bits value)	<b>500 *</b>
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

## 2.15. USART1

**Mode: Asynchronous**

### 2.15.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	<b>460800 *</b>
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### **Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 2.16. USART3

**Mode: Asynchronous**

### 2.16.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### **Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

\* User modified value

## 3. System Configuration

### 3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC3	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
	PA0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA6	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC2_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PB2	ADC2_IN12	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PB1	ADC3_IN1	Analog mode	No pull-up and no pull-down	n/a	VBUS
FDCAN1	PA11	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN2	PB12	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB8-BOOT0	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PA8	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PA9	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LPUART1_TX [STLINKV3E_VCP_RX]
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LPUART1_RX [STLINKV3E_VCP_TX]
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	T_SWCLK
TIM1	PC0	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC1	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC2	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	

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IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB14	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA5	TIM2_ETR	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PA4	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD2	TIM3_ETR	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC10	TIM8_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	TIM8_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC12	TIM8_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PC4	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1 [blue push button]
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	M2_EN
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	M1_EN

### 3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
ADC2	DMA1_Channel2	Peripheral To Memory	Low
ADC3	DMA1_Channel3	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	<b>Medium *</b>

#### ADC1: DMA1\_Channel1 DMA request Settings:

Mode: **Circular \***  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***

#### ADC2: DMA1\_Channel2 DMA request Settings:

Mode: Normal  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***

#### ADC3: DMA1\_Channel3 DMA request Settings:

Mode: Normal  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***  
 Peripheral Data Width: **Word \***  
 Memory Data Width: **Word \***

#### USART1\_TX: DMA1\_Channel4 DMA request Settings:

Mode: **Circular \***  
 Peripheral Increment: Disable  
 Memory Increment: **Enable \***

Peripheral Data Width: Byte  
Memory Data Width: Byte

### 3.3. NVIC configuration

#### 3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
ADC1 and ADC2 global interrupt		unused	
FDCAN1 interrupt 0		unused	
FDCAN1 interrupt 1		unused	
TIM1 break interrupt and TIM15 global interrupt		unused	
TIM1 update interrupt and TIM16 global interrupt		unused	
TIM1 trigger and commutation interrupts and TIM17 global interrupt		unused	
TIM1 capture compare interrupt		unused	
TIM2 global interrupt		unused	
TIM3 global interrupt		unused	
I2C1 event interrupt / I2C1 wake-up interrupt through EXTI line 23		unused	
I2C1 error interrupt		unused	
I2C2 event interrupt / I2C2 wake-up interrupt through EXTI line 24		unused	
I2C2 error interrupt		unused	
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25		unused	
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28		unused	

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM8 break interrupt			unused
TIM8 update interrupt			unused
TIM8 trigger and commutation interrupts			unused
TIM8 capture compare interrupt			unused
ADC3 global interrupt			unused
FPU global interrupt			unused
FDCAN2 interrupt 0			unused
FDCAN2 interrupt 1			unused
LPUART1 global interrupt			unused

### 3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true

\* User modified value



## 4. System Views

### 4.1. Category view

#### 4.1.1. Current

#### Middleware

#### System Core

#### Analog

#### Timers

#### Connectivity

#### Multimedia

#### Security

#### Computing

#### Utilities

DMA ✓

ADC1 ✓

TIM1 ✓

FDCAH1 ✓

GPIO ⚠

ADC2 ✓

TIM2 ✓

FDCAH2 ✓

NVIC ✓

ADC3 ✓

TIM3 ✓

I2C1 ✓

RCC ✓

TIM8 ✓

I2C2 ✓

SYS ✓

LPUART1 ✓

USART1 ✓

USART3 ✓

## 5. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32g4_bsd.zip">https://www.st.com/resource/en/bsdl_model/stm32g4_bsd.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32g4_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32g4_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32g4_svd.zip">https://www.st.com/resource/en/svd/stm32g4_svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-usb-c-pd-solutions-presentation.pdf">https://www.st.com/resource/en/product_presentation/stm32-usb-c-pd-solutions-presentation.pdf</a>
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Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32g4-series-product-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32g4-series-product-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32g4.pdf">https://www.st.com/resource/en/flyer/flstm32g4.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flpowerstbd.pdf">https://www.st.com/resource/en/flyer/flpowerstbd.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/fldpstpfc11120.pdf">https://www.st.com/resource/en/flyer/fldpstpfc11120.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf</a>

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